UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,698	03/05/2002	Brian N. Ripley	100202181-1	7441

7590	06/17/2004

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EXAMINER
INOA, MIDYS

ART UNIT	PAPER NUMBER
2188	10

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _04 June 2004_.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1-14,16-20 and 23-25_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) _1-14,16-20 and 23-25_ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on _03/05/02_ is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a) ☐ All   b) ☐ Some * c) ☐ None of:

      1. ☐ Certified copies of the priority documents have been received.

      2. ☐ Certified copies of the priority documents have been received in Application No. _____.

      3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   A request for continued examination under 37 CFR 1.114, including the fee set forth in

37 CFR 1.17(e), was filed in this application after final rejection. Since this application is

eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e)

has been timely paid, the finality of the previous Office action has been withdrawn pursuant to

37 CFR 1.114. Applicant's submission filed on June 1st, 2004 has been entered.

Claim Rejections - 35 USC § 102

2.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the

basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed
> in the United States before the invention by the applicant for patent or (2) a patent granted on an application for
> patent by another filed in the United States before the invention by the applicant for patent, except that an
> international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this
> subsection of an application filed in the United States only if the international application designated the United
> States and was published under Article 21(2) of such treaty in the English language.

3.   Claim1-14, 16-20, and 23-25 are rejected under 35 U.S.C. 102(e) as being anticipated by

Perego et al. (204/0019756 A1).

Regarding Claim 1, Perego et al. discloses a variable width memory system (300)

comprising a bus for communicating information (Figure 6A and 6B, Signal lines 645 and 650);

a plurality of variable width memory locations coupled to said bus, said variable width memory

locations having various bit widths to store information (PB0-PB7, Figure 3 and Page 2

paragraph 0031- Page 3 paragraph 034), wherein said plurality of variable width memory

locations receive a number of bits corresponding to the width of the variable memory locations

(bits received to fill a memory location is dependent on the width since the width specifies the

number of bits that a line can take before it is full); and a controller coupled to said bus (Figures

6A and 6B, 605), said controller directs access to said plurality of variable width memory locations. **Being that the memory has variable widths, the number of widths accessed depends of the current width of the memory location accessed. Configuration logic 310 determines which of the memory banks are selected through the acceptance of data bit signals (page 4, paragraph 0044-0048); the memory width is dependent on the configuration determined. Since configuration logic has the ability to change the current configuration of the system, the memory width from one access to the next can be different if the configuration has changed. Thus, the number of bits accessed can vary on a per access basis if the configuration and the width are different from one access to the next.**

Regarding Claim 2, Perego discloses variable width memory locations included on a single memory substrate (see Figure 3).

Regarding Claim 3, the memory of Perego's system could be a RAM, especially since it has similar components and behaves somewhat similarly to the RAM disclosed in Figure 2.

Regarding Claims 4-5, the memory locations of Perego have individual addresses and therefore, are identified by unique internal identifiers. These addresses are used by the controller in making access request. Additionally, such addresses can be part of a mapping system used at the time of access that can be implemented in the Row address buffer and refresh counter 225 and the Column address buffer and refresh counter 230 (see paragraph 0011).

Regarding Claim 6, in the system of Perego, two memory locations could have the same width depending on the parameters being used by the configuration logic 310 (paragraphs 0033-0034).

Regarding Claim 7, Perego discloses variably configuring the width of the memory in order to achieve a reduction in processor operations and power usage (paragraph 0031).

Regarding Claim 8 and 14, Perego et al. discloses a variable width memory (300) comprising receiving a register indicator corresponding to a register (Mode register 220); accessing a memory cell (one of memory banks PB0-PB7) based on said register indicator, wherein said memory cell is allocated a storage size correlating to the bit capacity of said register (Paragraph 0012); and transferring information between said memory cell and another component (controller 605), wherein said information includes the same number of bits as said bit capacity. **Being that the memory has variable widths, the number of widths accessed depends of the current width of the memory location accessed. Configuration logic 310 determines which of the memory banks are selected through the acceptance of data bit signals (page 4, paragraph 0044-0048); the memory width is dependent on the configuration determined. Since configuration logic has the ability to change the current configuration of the system, the memory width from one access to the next can be different if the configuration has changed. Thus, the number of bits accessed can vary on a per access basis if the configuration and the width are different from one access to the next.**

Regarding Claims 9-10, the indicator in register 220 is dependent on a command received by control logic 215 from processor 605 (Paragraph 0008). In this case, the command that the control logic 215 receives is a processing criteria associated with a processor.

Regarding Claim 11, information is often transferred in the form of packets; therefore, such information being transferred to and from the memory could be in the form of a packet; where a packet can be a group of bits or bytes of information.

Regarding Claim 12, the information being transferred to and from the memory also includes information such as column access enable, row access enable, and write commands. These commands are associated with certain fields in the memory that perform certain functions this completing such commands (see Figure 3).

Regarding Claim 13, the information being transferred that is associated with certain fields is sequentially received and taken in by the command decoder 210 within the memory 300 (see Figure 3).

Regarding Claim 20, Perego et al. discloses a variable memory width assignment method (paragraphs 0031-0034) comprising analyzing a data block configuration specification (from mode register 220); identifying bits in a portion of said block of data, wherein said portion corresponds to information grouped in an arrangement that facilitates reduction of processing instructions; and assigning a memory location width equal to said number of bits in said portion of said block of data (paragraphs 0012 and 0033-0034), wherein said data block is arranged in accordance with a communication packet configuration specification. Since information is often transferred in the form of packets; data blocks being transferred to and from the memory could be in the form of a packet; where a packet can be a group of bits or bytes of information. Therefore, in assigning the width of a memory location, the size of a packet is also being configured. **Being that the memory has variable widths, the number of widths accessed depends of the current width of the memory location accessed. Configuration logic 310**

determines which of the memory banks are selected through the acceptance of data bit signals (page 4, paragraph 0044-0048); the memory width is dependent on the configuration determined. Since configuration logic has the ability to change the current configuration of the system, the memory width from one access to the next can be different if the configuration has changed. Thus, the number of bits accessed can vary on a per access basis if the configuration and the width are different from one access to the next.

Regarding Claims 16-18, as in all memories, the variable width memory of Perego et al. has many memory locations uniquely identified by memory addresses, which could be known as external identifiers.

Regarding Claim 19, Perego et al. discloses a variable width memory system, which inherently arranges the width bits in a contiguous manner in order to provide easier access.

Regarding Claim 23, Perego et al. discloses a variable width memory assignment system (300) comprising a means for communicating memory location identifiers (addresses communicated through Signal lines 645 and 650 and inputted into the memory system through I/O buffer 325); a means for storing information in a uniquely identifiable different width memory locations corresponding to said memory location identifiers (PB0-PB7, Figure 3 and Page 2 paragraph 0031- Page 3 paragraph 034), wherein said means for storing said information returns a number of bits equal to the width of one of said uniquely identifiable different width memory locations in response to a read request (read data is returned to data control circuit 315 which then routes data to the I/O buffer so that it may be provided to the requestor, Figure 3, Page 3 paragraph 0034); and a means for managing a connection with said uniquely identifiable different width memory locations (data control circuit 315, Figure 3), wherein said means for

managing said connection supervises writing and reading of information to and from said

uniquely identifiable different width memory location. **Being that the memory has variable**

widths, the number of widths accessed depends of the current width of the memory

location accessed. Configuration logic 310 determines which of the memory banks are

selected through the acceptance of data bit signals (page 4, paragraph 0044-0048); the

memory width is dependent on the configuration determined. Since configuration logic has

the ability to change the current configuration of the system, the memory width from one

access to the next can be different if the configuration has changed. Thus, the number of

bits accessed can vary on a per access basis if the configuration and the width are different

from one access to the next.

Regarding Claim 24, Perego et al. discloses a memory assignment system (300) wherein

said means for managing said connection (315) includes a means for tracking a correspondence

(data routing logic, Page 3, paragraph 0034) between said uniquely identifiable variable widths

memory (305) and register identifiers (320).

Regarding Claim 25, Perego et al. discloses a variable width memory assignment system (300)

wherein said register identifiers (320) are provided by a means for processing said information

(Page 3, paragraph 0039).

Response to Arguments

4.   Applicant's arguments filed on June 04, 2004 have been fully considered but they are not

persuasive. Applicant argues that Perego does not teach or suggest "wherein said number of bits

potentially varies on a per access basis depending on which variable width memory location of

said plurality of variable width memory locations is being accessed". However, Perego discloses

that configuration logic determines the number of memory banks to be selected and depending

on this determination, the device width is selected. Therefore, the memory width can be changed

if the configuration is changed (Page 4, paragraph 0047). The memory width depends on the

memory bank configuration and **being that the memory has variable widths, the number of**

widths accessed depends of the current width of the memory location accessed.

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Midys Inoa whose telephone number is (703) 305-7850. The

examiner can normally be reached on M-F 7:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for

the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Midys Inoa
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Art Unit 2188

MI

6/14/07

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SUPERVISORY PATENT EXAMINER